WBS 3.1.2 - Calorimeter Trigger

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Level-3 Project Manager

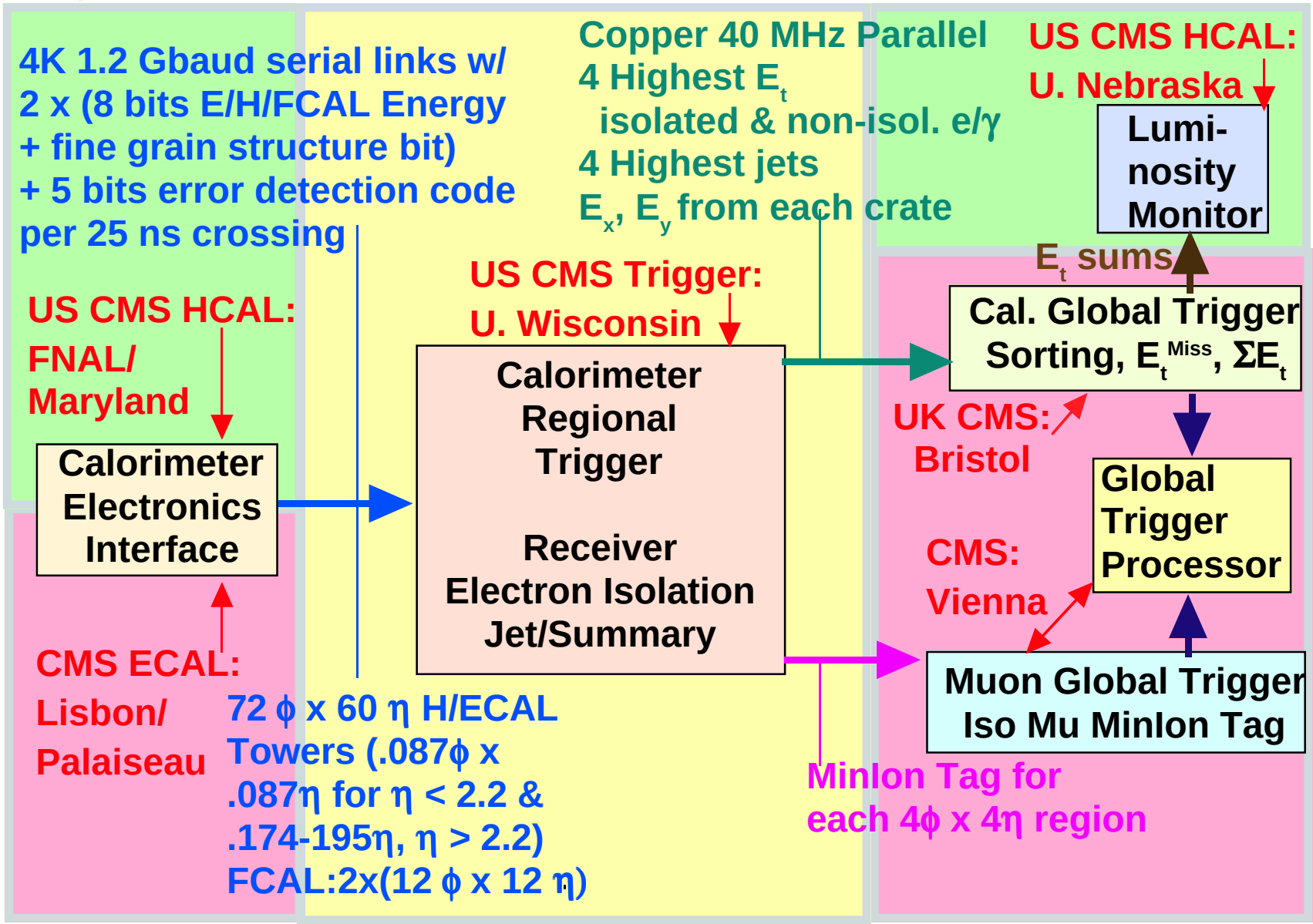
CMS Calorimeter Trigger Project

University of Wisconsin

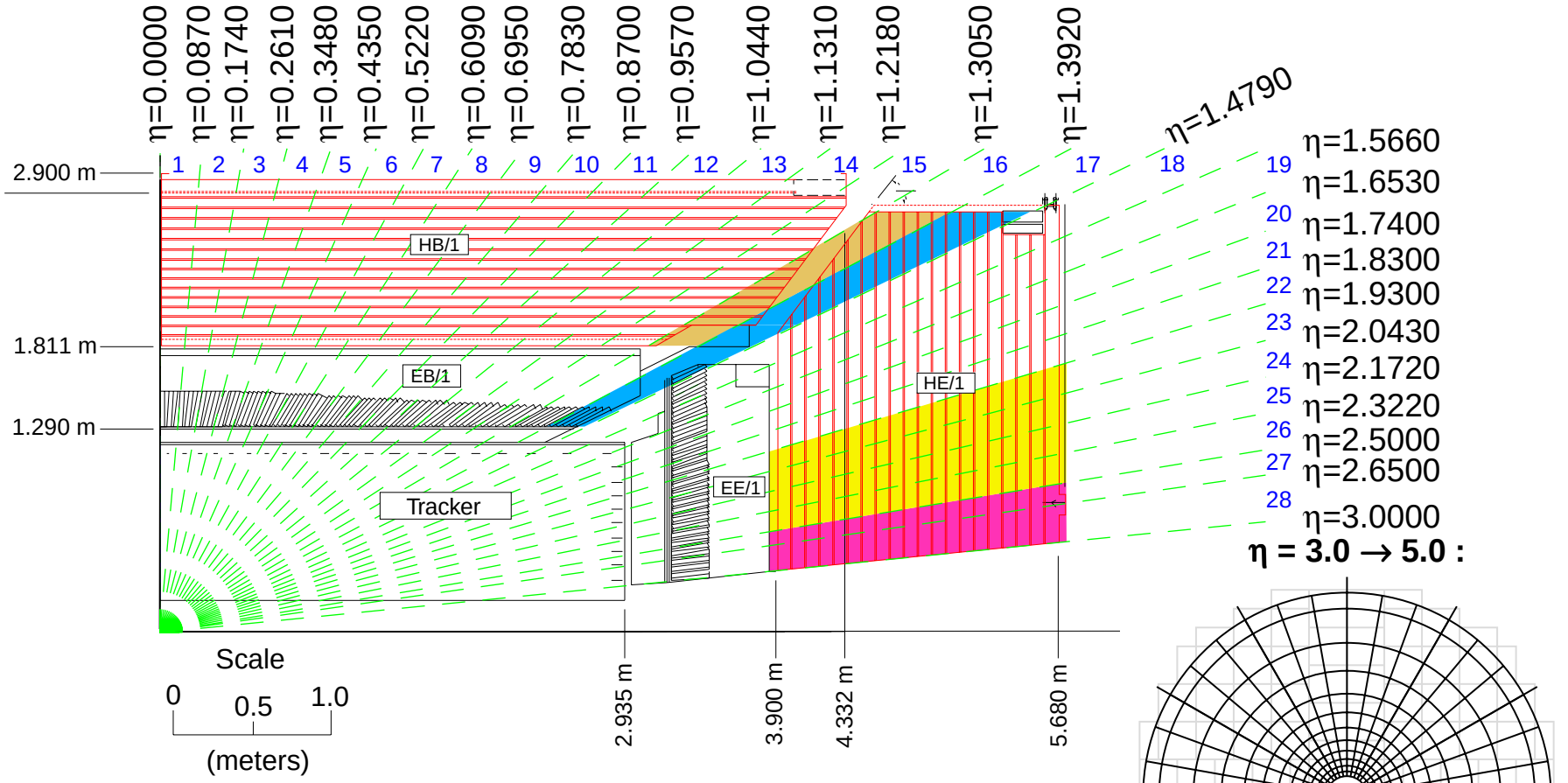
DOE/NSF Review

May 9, 2000

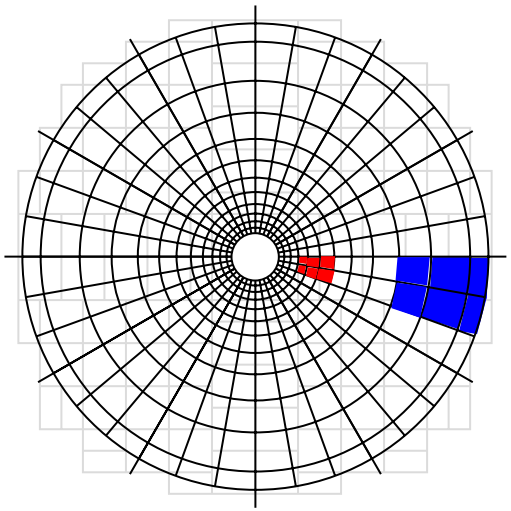
Calorimeter Trigger Overview



Calorimeter Trigger Geometry



η = 3.0 → 5.0 :

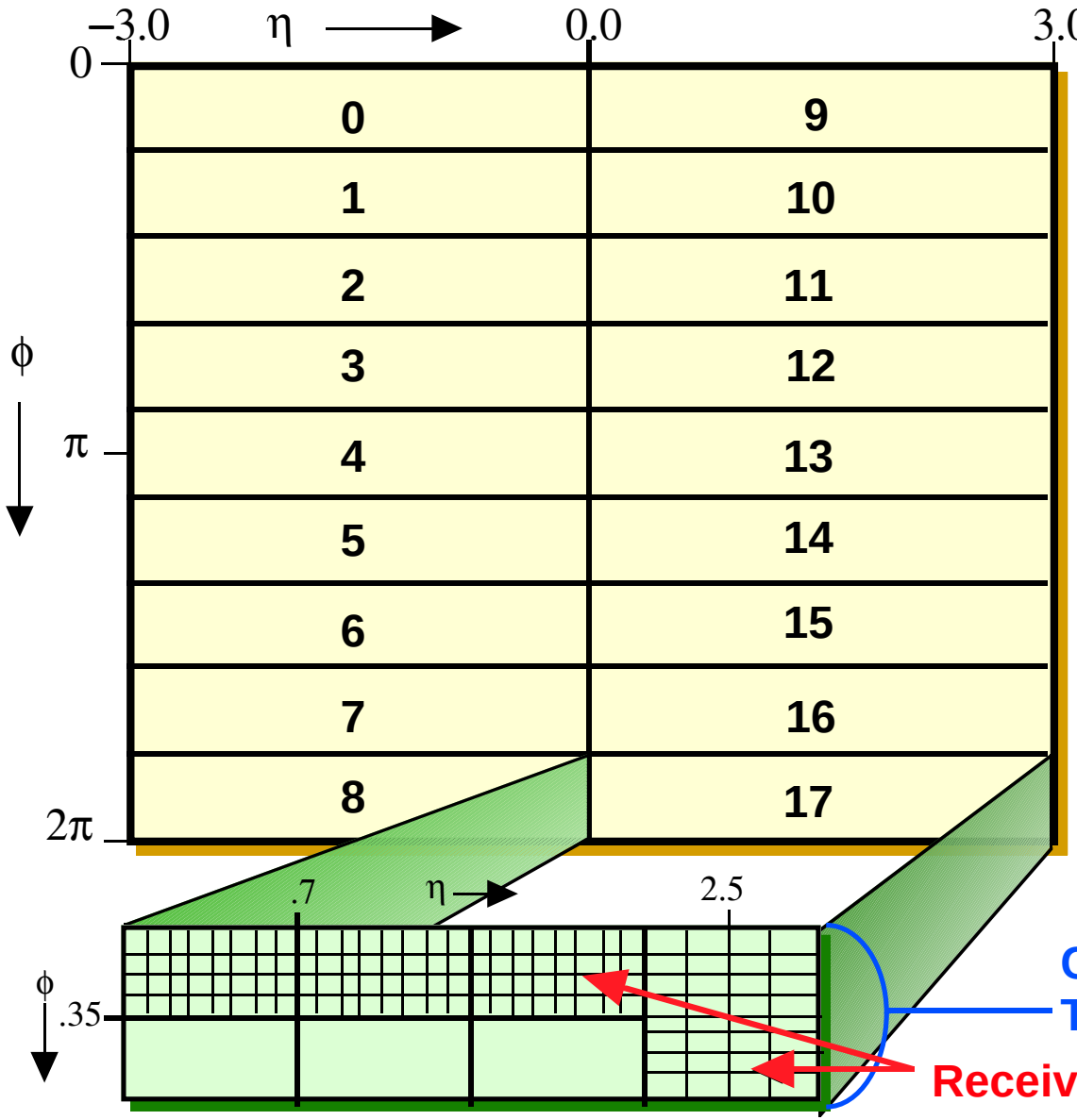


2 CMS HF Calorimeters mapping onto Trigger System HF Crate

Readout segmentation: 36ϕ × 12η × 2z × 2F/B

Trigger Tower segmentation: 18ϕ × 4η × 2F/B

Cal. Trigger Tower Mapping



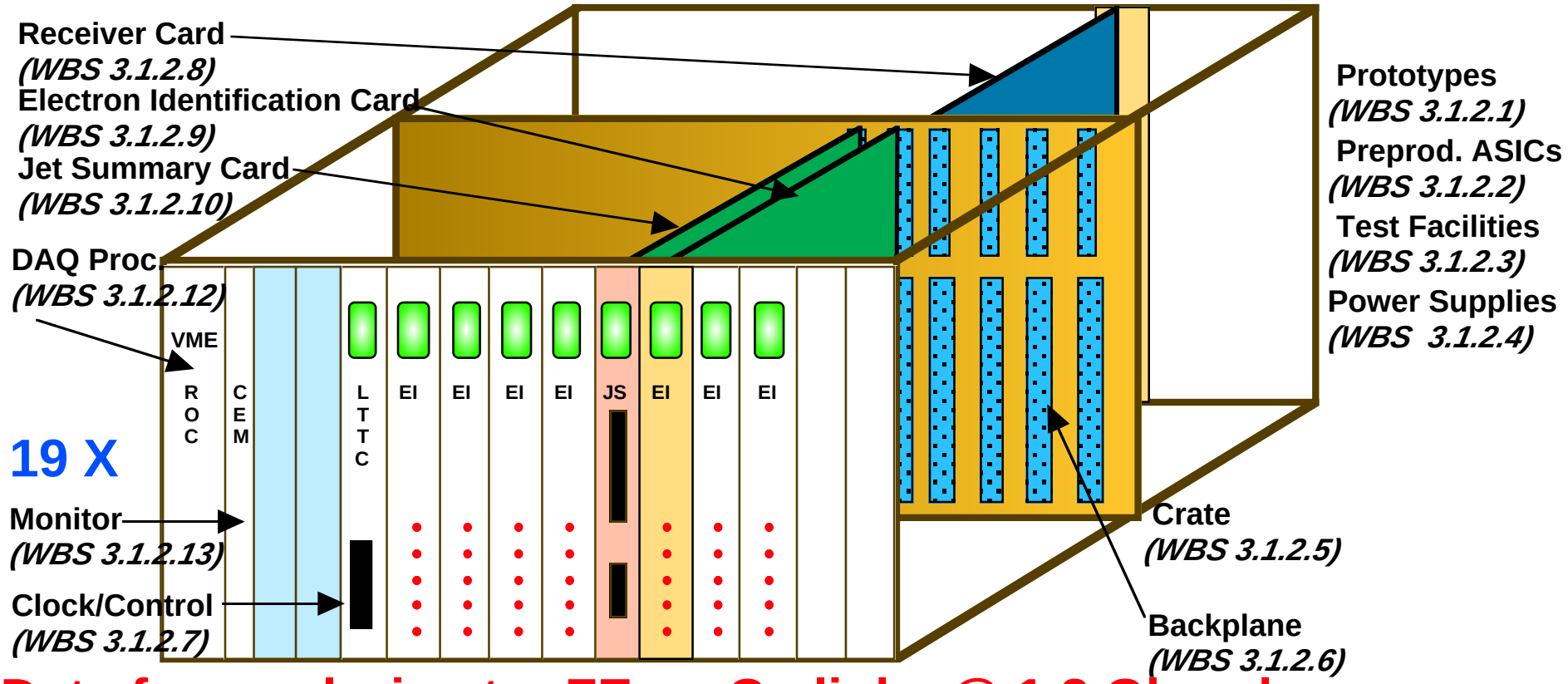
18 crates for barrel & endcap calorimeters + 1 for v. forward.

Each crate processes a 0.7 ϕ x 3.0 η region.

Each Receiver/Elec. ID card pair typically covers a .35 ϕ x 0.7 η region (modifed in high-η endcap region)

Regional Calorimeter Crate

(WBS 3.1.2)



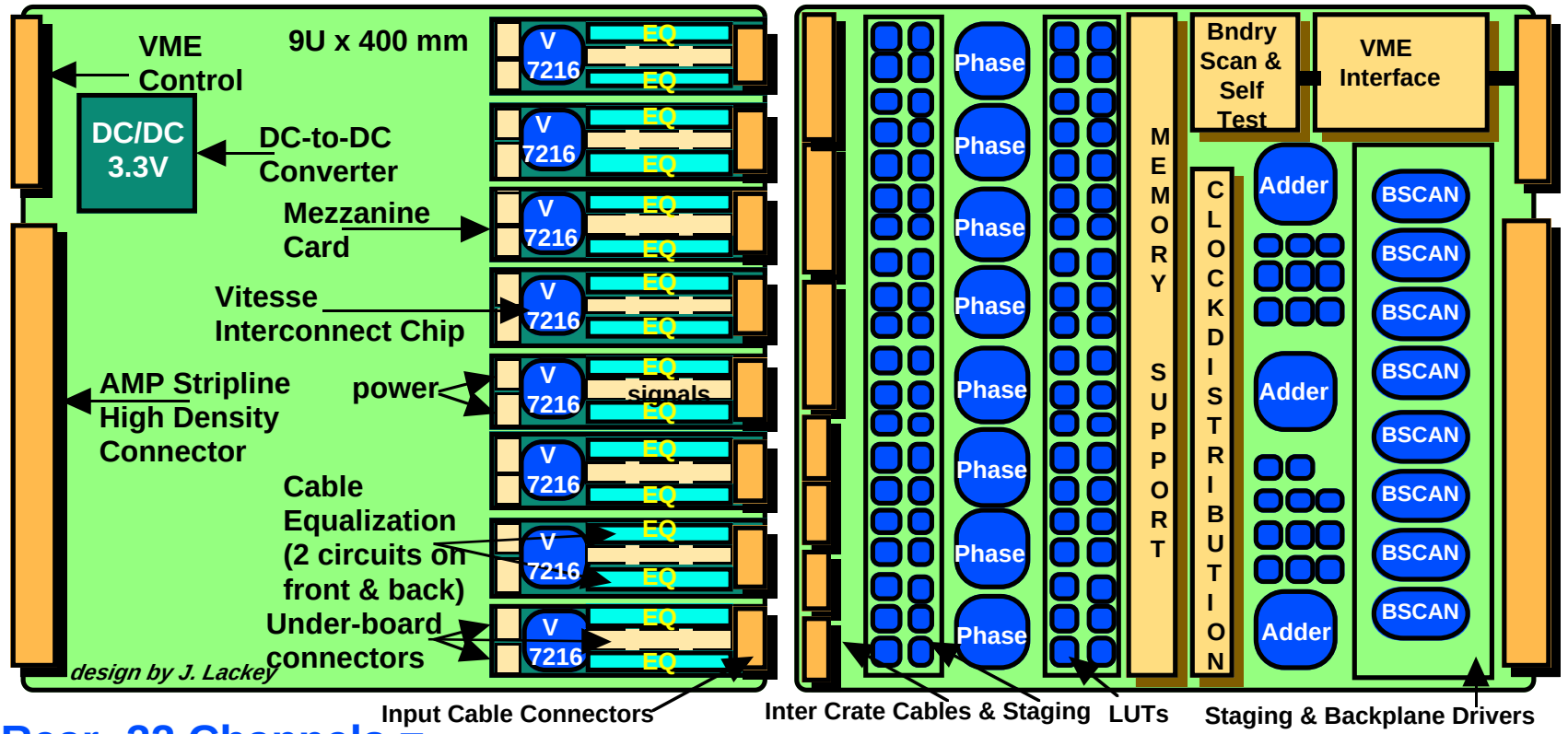
Data from calorimeter FE on Cu links @ 1.2 Gbaud (ptyp. tstd.)

- Into 133 rear-mounted Receiver Cards (ptyp. tstd. w/ ASICs)

160 MHz point to point backplane (ptyp. tstd.)

- 19 Clock&Control (ptyp. tstd.), 133 Electron ID (ptyp. tstd.)
  19 Jet/Summary, Receiver Cards operate @ 160 MHz

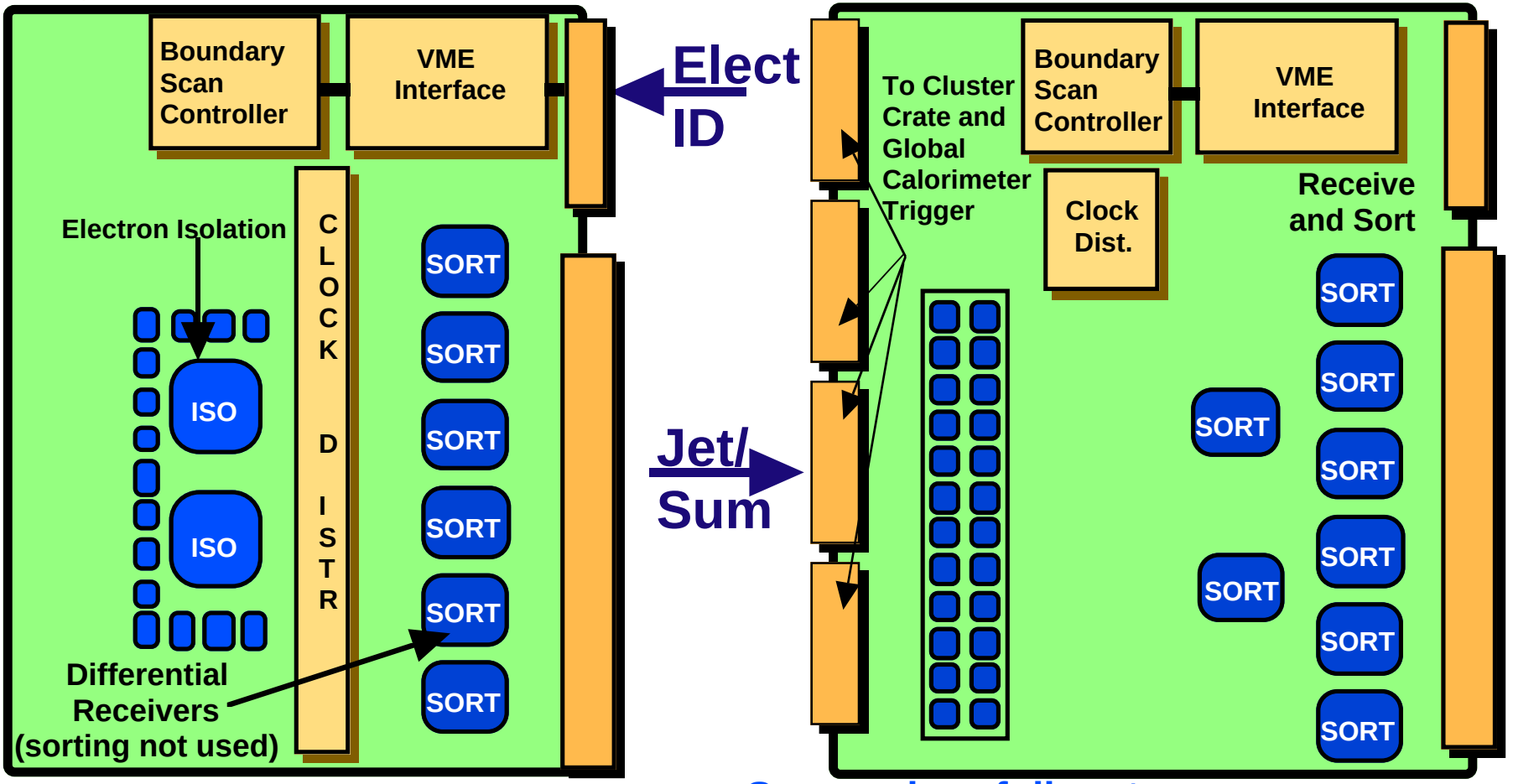
Receiver Card



Rear: 32 Channels =
4 Ch. x 8 mezzanine cards
1.2 GBaud copper rcvrs
18 bit (2x9) data + 5 bit error
Vitesse Chip:
Converts Serial to Parallel
Data to front at 120 MHz TTL

Front: Phase ASIC: Deskew,Mux @ 160MHz
Error bit for each 4x4, Test Vectors
Memory LUT @ 160 MHz
Linearization and e/γ & τ veto bits
Adder ASIC:
8 inputs @ 160 MHz in 25 ns.
Differential Output@160 MHz

Electron ID & Jet/Summary Cards



Processes 4x8 region @ 160 MHz
Electron isolation on ASIC
Lookup tables for ranking
Takes Max in each 4x4

Summarizes full crate:
Sorts 14 iso. e's → top 4 iso e's
Sorts 14 non. iso e's → top 4 non iso e's
Stages 4x4 E_T sums to cluster crate
Iso, non iso e's and Quiet/MinI bits to GCT

Jet/τ Cluster and HF Crates

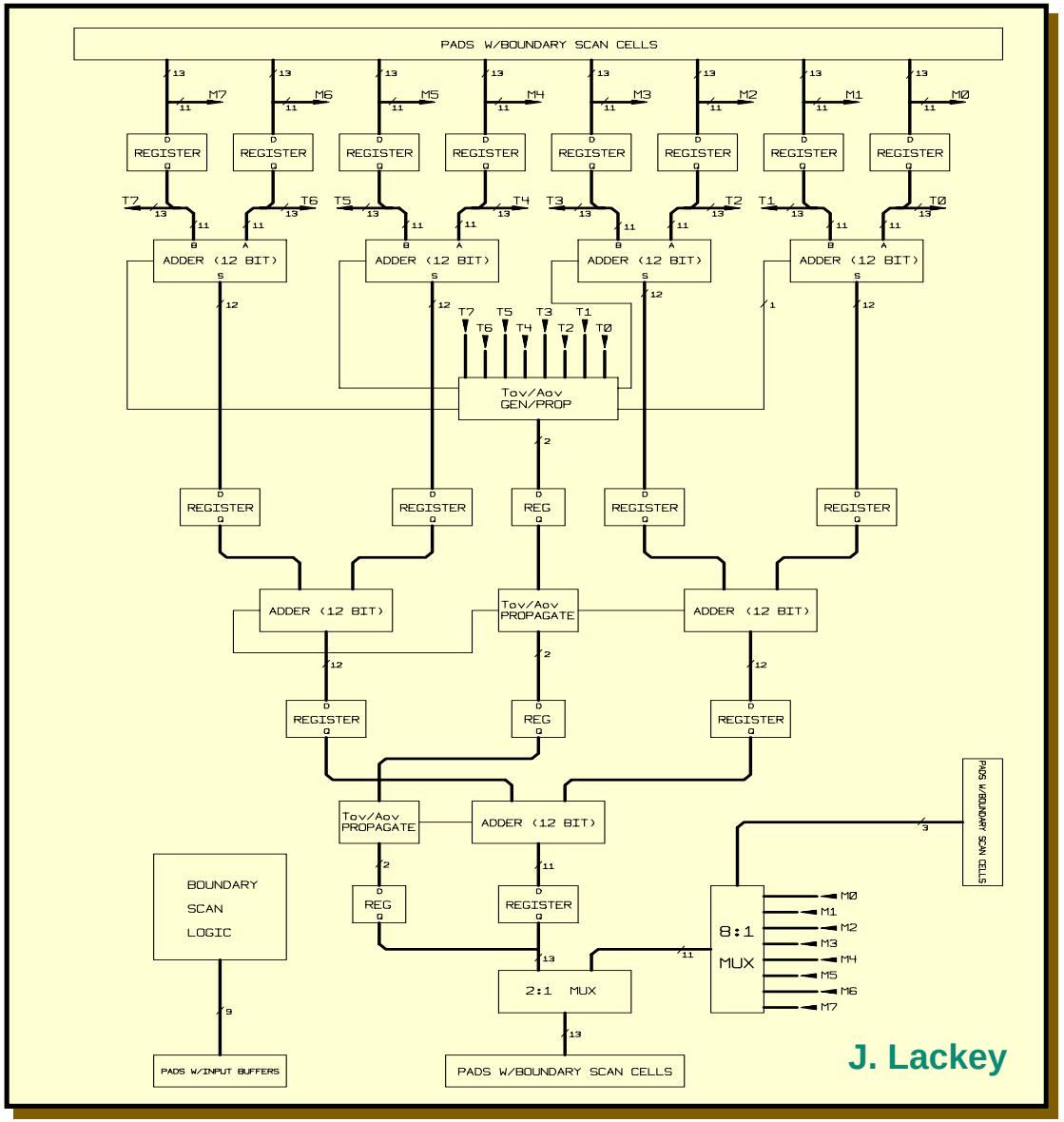
Jet/τ Clustering

- **New algorithms to seamlessly cover all η–ϕ**
  - New CMS physics requirement
- **HF Crate**
  - Uses portion of Receiver and Jet/Summary card functions
    - **Vitesse serial links**
    - **Look Up Tables for linearization**
    - **Drive parallel differential signals to external crate**
  - May be able to integrate in Jet/Summary card
- **Cluster Crate with proven RCT technology**
  - Parallel differential signal input for all η–ϕ
  - Custom backplane for data sharing
  - Reuse ADDER, BSCAN & SORT ASICs for processing
  - All ECL logic with 160 MHz processing

8 x 13-bit 160 MHz Adder ASIC

Vitesse 0.6µ H-GaAs
Process: ECL I/O

- 13 bits per operand
  x 8 operands
- Thirteen bit output
- Latency:
  25 ns @ 160 MHz
- Full Boundary Scan
- ~11,000 cells
- 4 Watts
- Tested > 200 MHz
- Operated on RC
- In Production



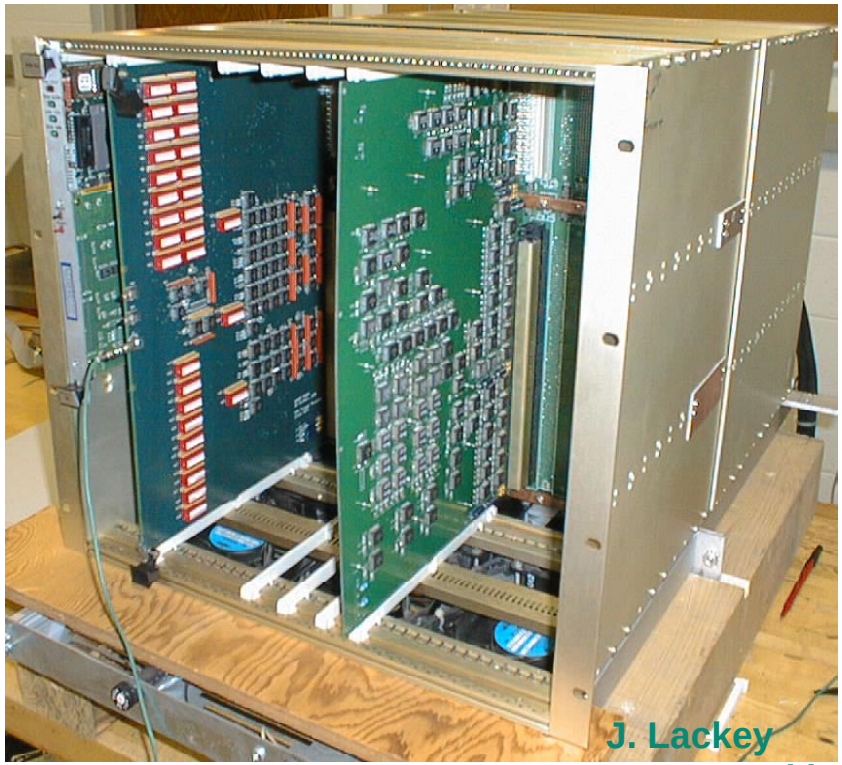
Cal. Trigger Dataflow Test

Prototype Crate with

- **160 MHz Backplane**
- **Proto. Receiver Card (rear)**
- **Proto. Clock Card (front)**
- **Proto. Electron ID Card (front)**

Full 160 MHz dataflow verified

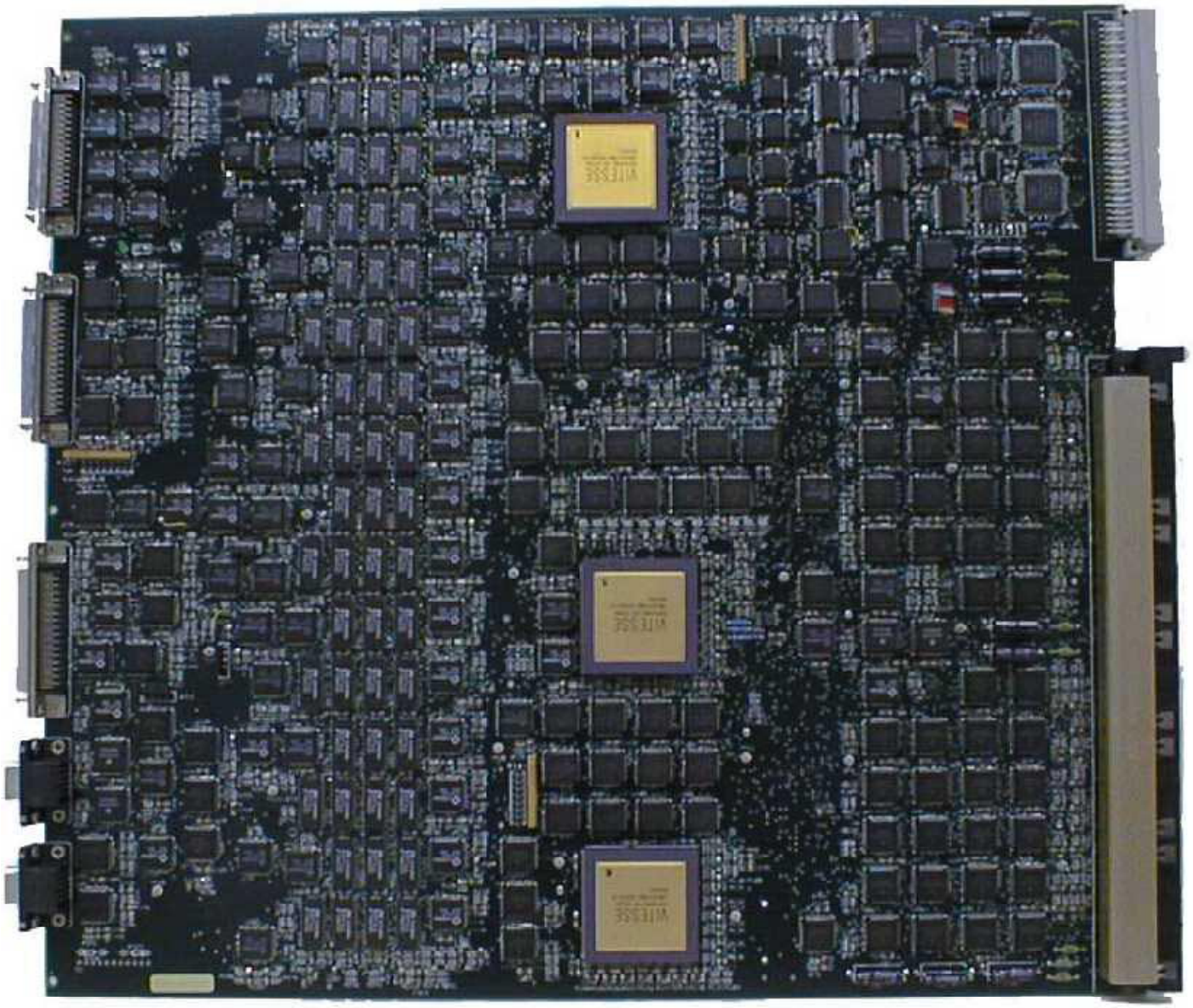
REAR



FRONT

J. Lackey
M. Jaworski

Prototype Receiver Card



160 MHz Prototype Receiver Card tests:

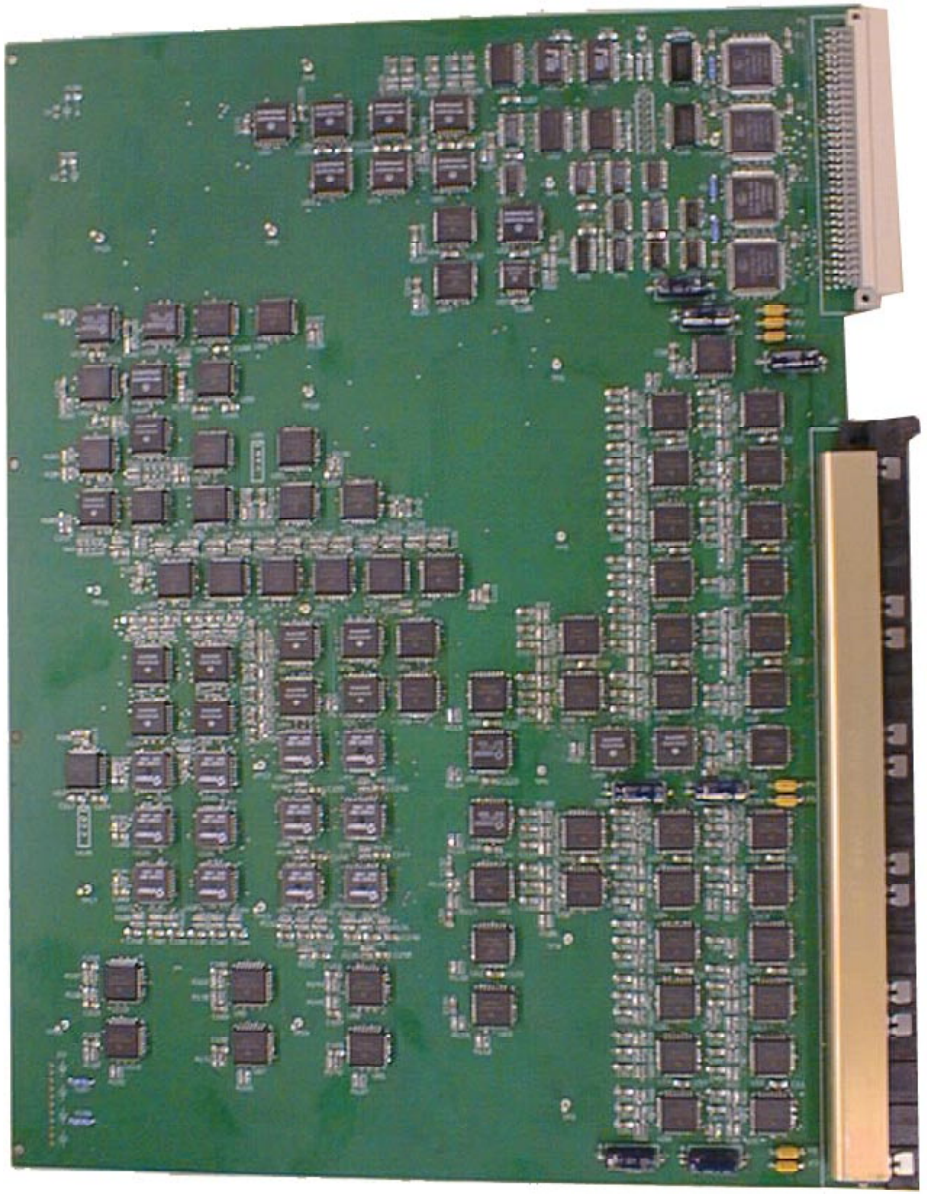
- VME Interface checked
- Adder ASIC's checked
- Timing checked
- Intercrate sharing checked

J. Lackey

Electron ID Card Prototype

Card tested:

- VME Interface working
- Dataflow from Receiver Card through custom backplane works
- Timing checked
- Logic verified



J. Lackey

ASIC Development - I

Prototype Phase ASIC (Receiver Card)

J. Lackey

- Input: 120 MHz TTL data from Gbit Link Mezzanine Card
- Output: 160 MHz ECL data & error detection
- Status:
  - Full speed tests by Vitesse passed
  - Prototypes in hand for testing on our RC

Prototype Boundary Scan ASIC (Receiver Card)

- Boundary scan of Receiver Card Input
- Backplane drivers -- compact circuitry
- Status:
  - Full speed tests by Vitesse passed
  - Prototypes in hand for testing on our RC

Both ASICs placed on new Receiver Prototype

ASIC Development - II

Electron ID ASIC (Electron ID Card) J. Lackey

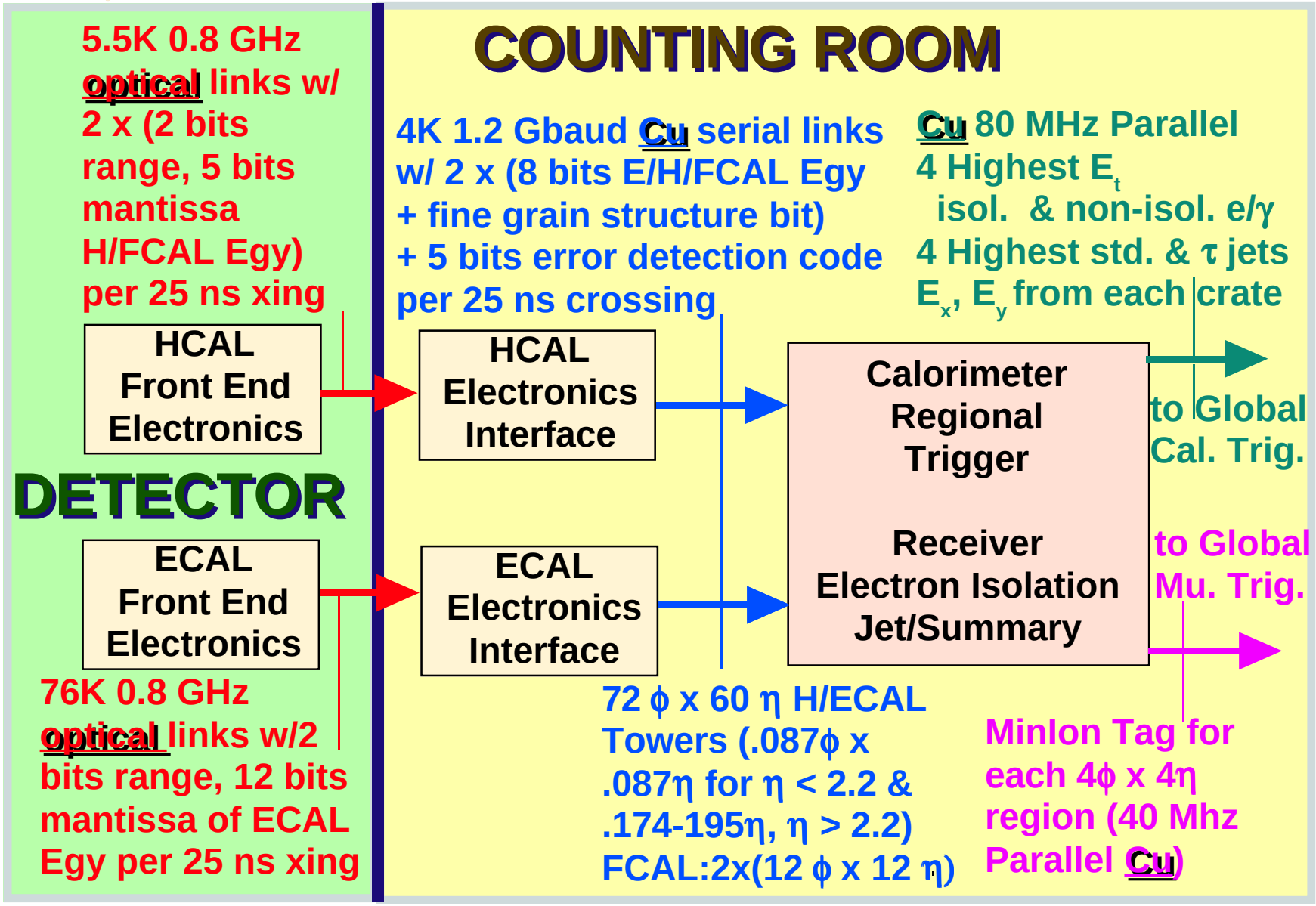
- **Implements Electron Isolation algorithm**
  - Described in talk of P. Chumney
- **Status**
  - Full speed tests by Vitesse passed
  - Prototypes in hand for testing on EIC

Sort ASIC (EID & Jet/Summary Card)

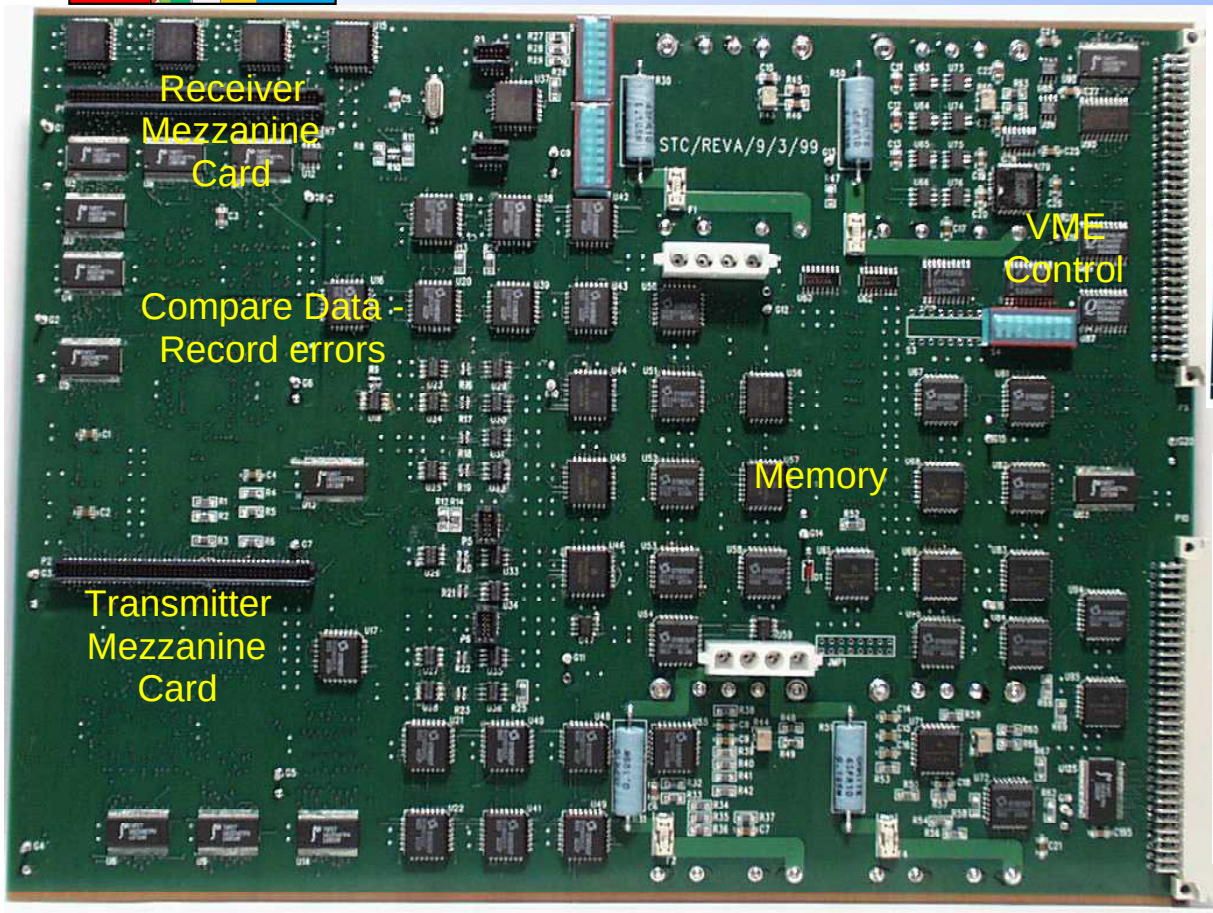
- **Integrated backplane receivers & sorting**
  - Passes 4 highest rank of 32 inputs
  - Sorts input before passing unto card
- **Status**
  - Full speed tests by Vitesse passed
  - Prototypes in hand for testing on EIC

Will test with new Electron ID Card prototype

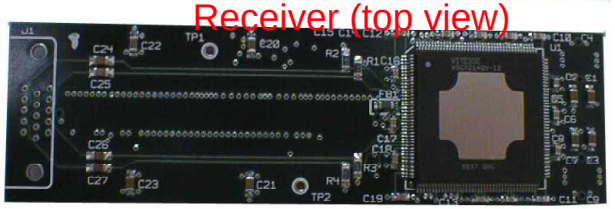
Calorimeter Trigger Links



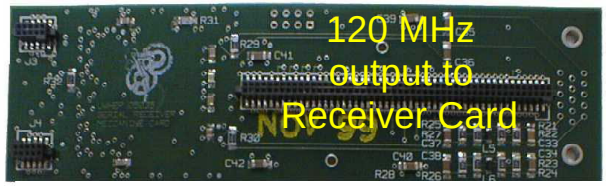
Copper Cable Gbit Serial Data Tests



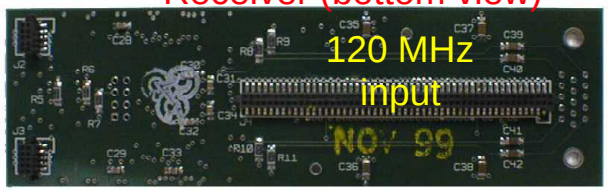
Receiver (top view)



Transmitter (top view)



Receiver (bottom view)



Transmitter (bottom view)

Serial Link Test Card includes VME, memories & comparison circuitry to fully test serial links @ 120 MHz TTL from Mezzanine Cards. (U. Wisconsin)

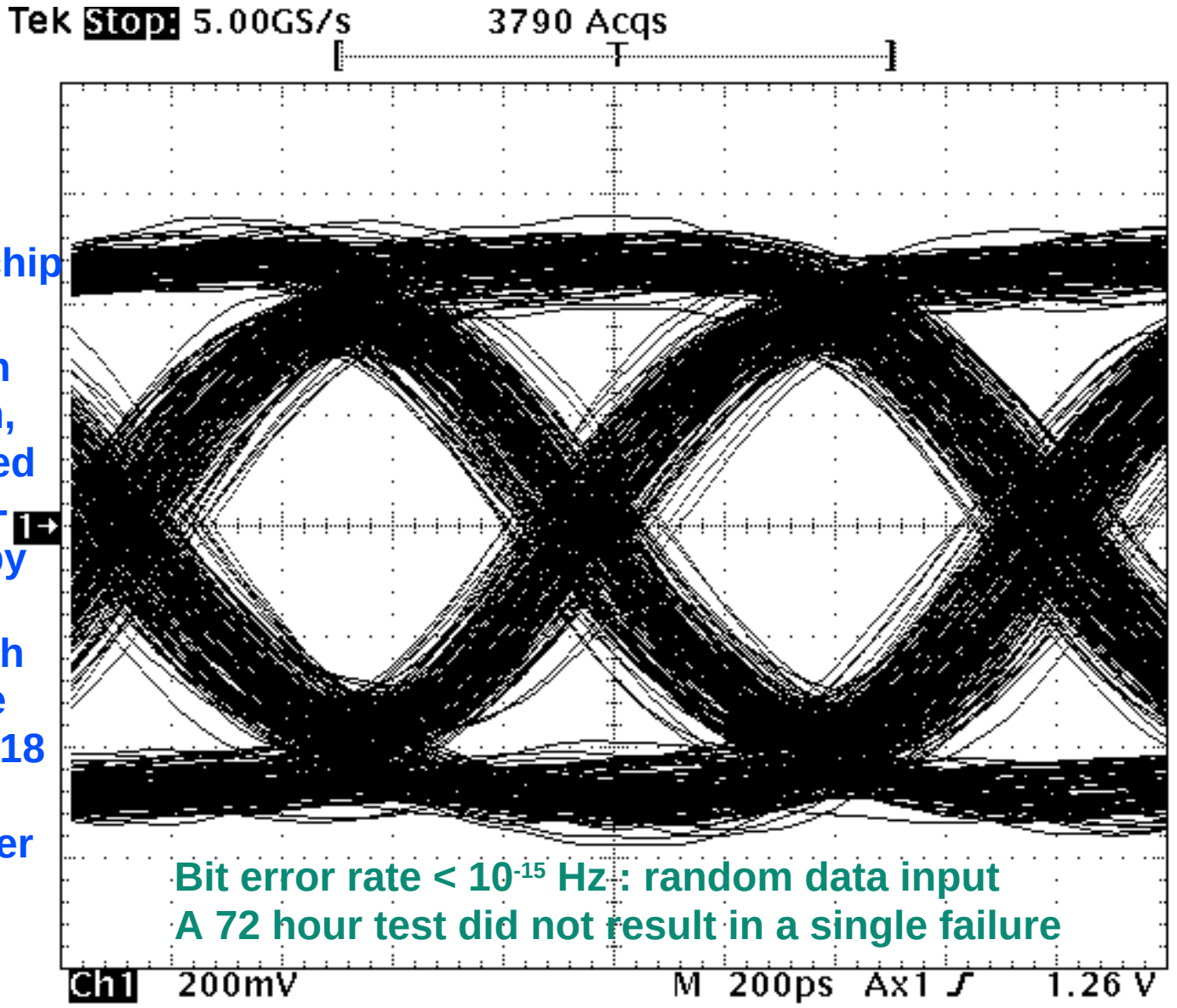
Mezzanine Transmit & Receive Cards convert 4 x 1Gb/s links to 120 MHz TTL w/ Vitesse 7214 & cable equalization

J. Lackey
P. Robl
D. Wahl

GBit Data Transmission

Tests over 20 m copper cable

- **Vitesse 7214 4 x Gigabit Interconnect chip**
- **twisted pair cables (Belden 9182 (150 ohm, 22AWG, foamed dielectric,twin-ax) grouped by fours & terminated with 8-pin DIN style connectors $318 per 500 foot spool ($2.10 per meter).**



Bit error rate < 10^{-15} Hz : random data input
A 72 hour test did not result in a single failure

J. Lackey
P. Robl

Trigger Link Bit Error Detection

Link error code simulation:

- **Between ECAL & HCAL Upper Level Readout & Cal. Regional Trigger**
  - 2x(8 bits E_T + 1 bit finegrain) + 5 bits error detection code* + 1 bit "Gap Flag" = 24 bits/25 ns
  - Full 5-bit Hamming Code* finds all 1 & 2-bit errors (most common)
  - Also finds more than 96% of any other error type
- **Procedure upon error is to zero and log the error for readout by DAQ**
- **Full implementation in Phase ASIC**
  - Now integrated in Receiver card

Bits with errors	Number of Patterns	Percent of Errors not found
0	1	0.00
1	24	0.00
2	276	0.00
3	2024	3.45
4	10626	3.49
5	42504	3.03
6	134596	0.08
7	346104	0.17
8	735471	0.06
9	1307504	0.14
10	1961256	0.01
11	2496144	0.01
12	2704156	0.02
13	2496144	0.01
14	1961256	0.10
15	1307504	0.15
16	735471	0.06
17	346104	0.30
18	134596	0.08
19	42504	3.24
20	10626	3.23
21	2024	2.77
22	276	0.03
23	24	0.00
24	1	0.00

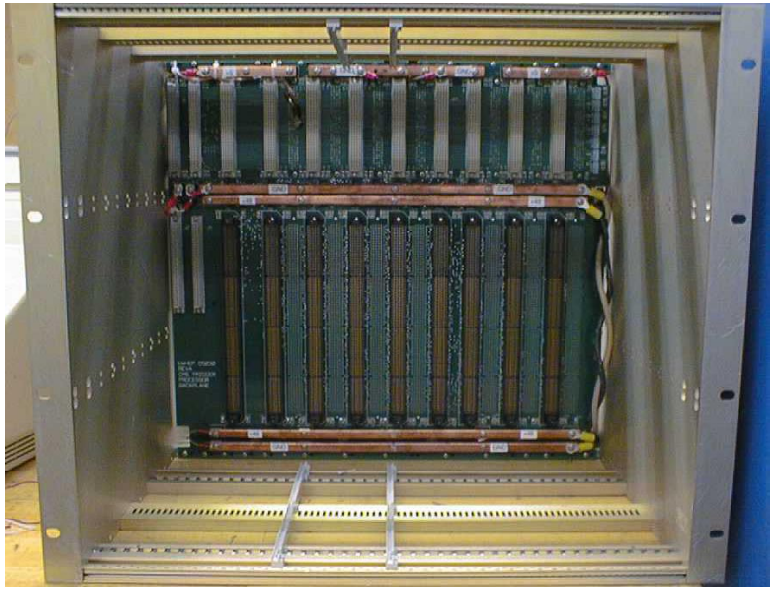
Second Generation Prototypes

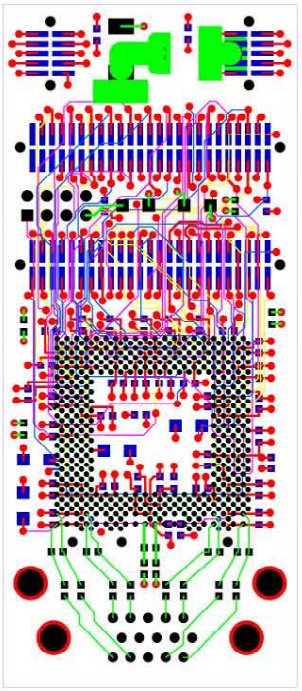
Ready for tests

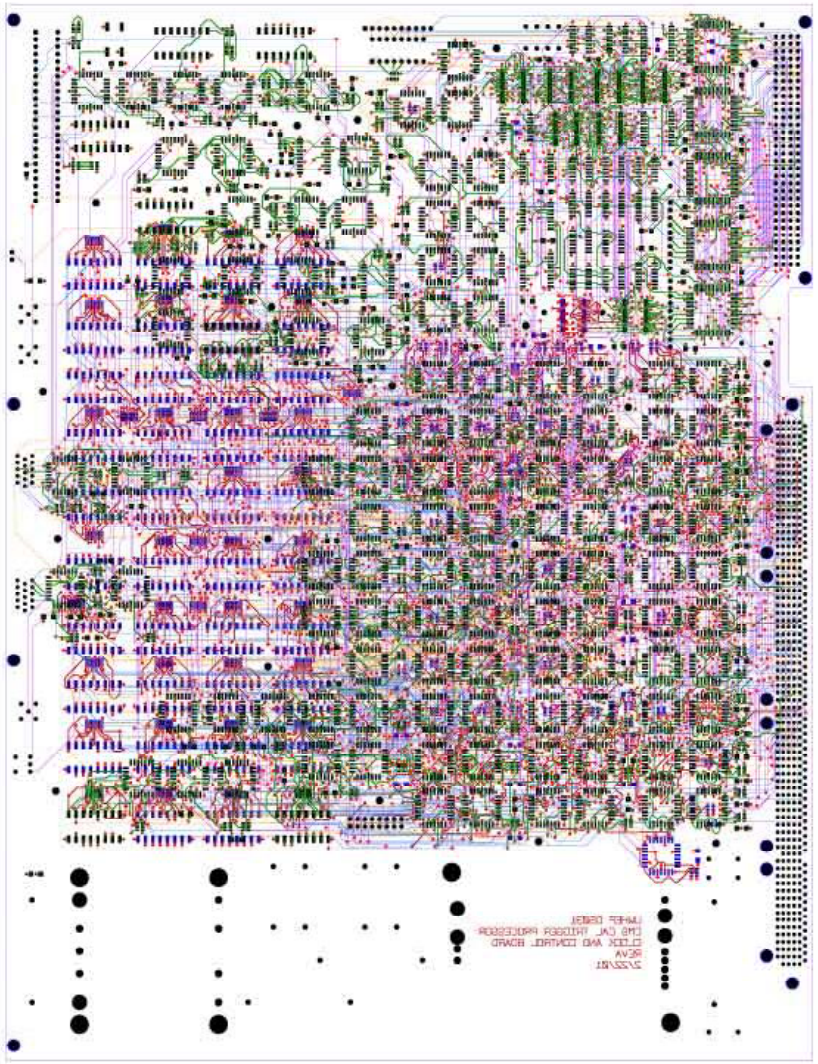
- Crate & Backplane

Ready for manufacture

- Clock & Control
- Serial Link mezzanine cards







Plans for This Year

Crate & Backplane

- Ready for summer tests
- Assemble production versions after validation in summer

Serial Links

- Finish new Serial Test Card (STC) for integration with E,HCAL
- New Mezz. card (w V7216) detailed validation on STC

ASIC Procurement

- Complete order from Vitesse after summer tests

Clock & Control, Receiver (RC) and Electron Isolation Cards (EIC)

- Finish design and manufacture 2nd generation prototypes
- Validate Serial Links, Phase & Boundary Scan ASICs on RC
- Validate Sort & Electron ID ASICs on EIC

Jet/Summary Card

- Design first prototype - including output to cluster crate

Cluster and HF crates

- Finalize designs

Cal Trigger Personnel

Physicists (at Wisconsin)**:**

- **Faculty: W. Smith & S. Dasu**
- **Ph.D. Physicists: P. Chumney & F. Di Lodovico**

Engineers (experienced team at Wisconsin)**:**

- **J. Lackey -- Lead Engineer & Designer**
  - Also Lead Engineer for Zeus Calorimeter Trigger
- **M. Jaworski -- Board Layout & Design support**
  - Worked on Zeus Calorimeter Trigger
- **R. Fobes -- Procurement and Assembly**
  - Worked on Zeus Calorimeter Trigger
- **P. Robl -- Copper Links & Design support**
  - PSL Engineer, assisted by lead PSL electronics engineer, D. Wahl, who worked on Zeus Trigger

Cal Trigger Production and Testing

Electronics testing and remediation of manufacturing defects

- **J. Lackey - Lead Engineer**
- **M. Jaworski, R. Fobes - Engineering Support**
- **P. Chumney - In charge of testing**

Software development (for tests and operation)

- **Need professional team with real-time programming skills**
  - Good post-doctoral project
  - CS or EE or suitably qualified physics graduate students

Personnel is a concern

- **Will need more people for production testing and software support**
  - P. Chumney works on hardware at 50% level
    - **Will supervise testing and develop software**
  - Work with S. Dasu who has teaching responsibility now
  - Will need a crew for testing
    - **ZEUS used 2 post-docs, 4 students for 2 years**
- **Base program support for post-doc and students necessary**

Conclusions

Status

- **Ready to test 2nd generation prototypes in summer**
  - Crate and Backplane ready
  - ASICs ready, other parts procured
  - Clock & Control and Receiver Cards in final design
  - Electron Isolation Card in design
  - Serial Link Mezzanine Cards ready
  - Serial Link Test Card in final design

Goals for this year

- **Complete of prototype tests, validate & order ASICs**
- **Integrate Serial Links with ECAL,HCAL front-end**
- **Finalize Jet/Summary card design**